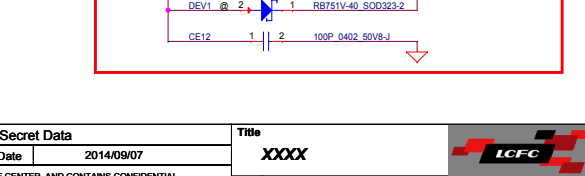
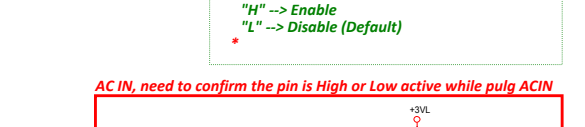
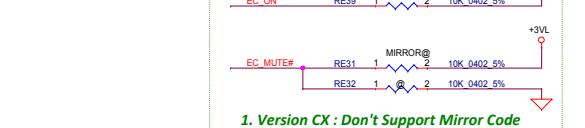
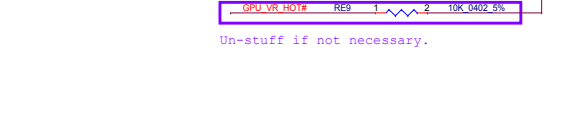
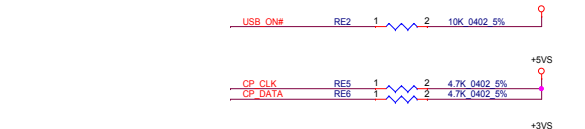
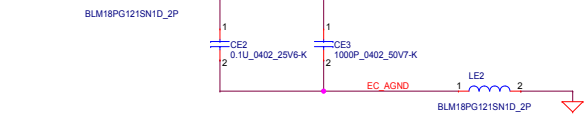
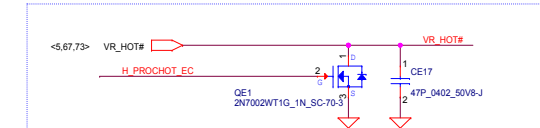


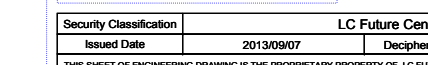
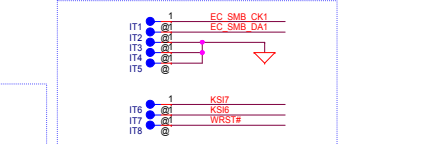
Board ID	RE7	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	Phase
0	0K +/- 5%	0 V	0 V	0 V	Pre-SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SVT
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



**PROCHOT#**  
 (EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)

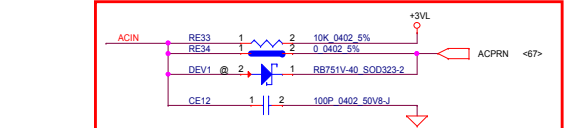


**For factory EC flash**



1. Version CX : Don't Support Mirror Code  
 Version DX/EX/FX : Support Mirror Code  
 "H" --> Enable  
 "L" --> Disable (Default)

AC IN, need to confirm the pin is High or Low active while pulg ACIN



Security Classification	LC Future Center Secret Data	Title
Issued Date	2013/09/07	Deciphered Date
Deciphered Date	2014/09/07	2014/09/07
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Size	Document Number	Rev
C	AITE1 NM-A221	1.0
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