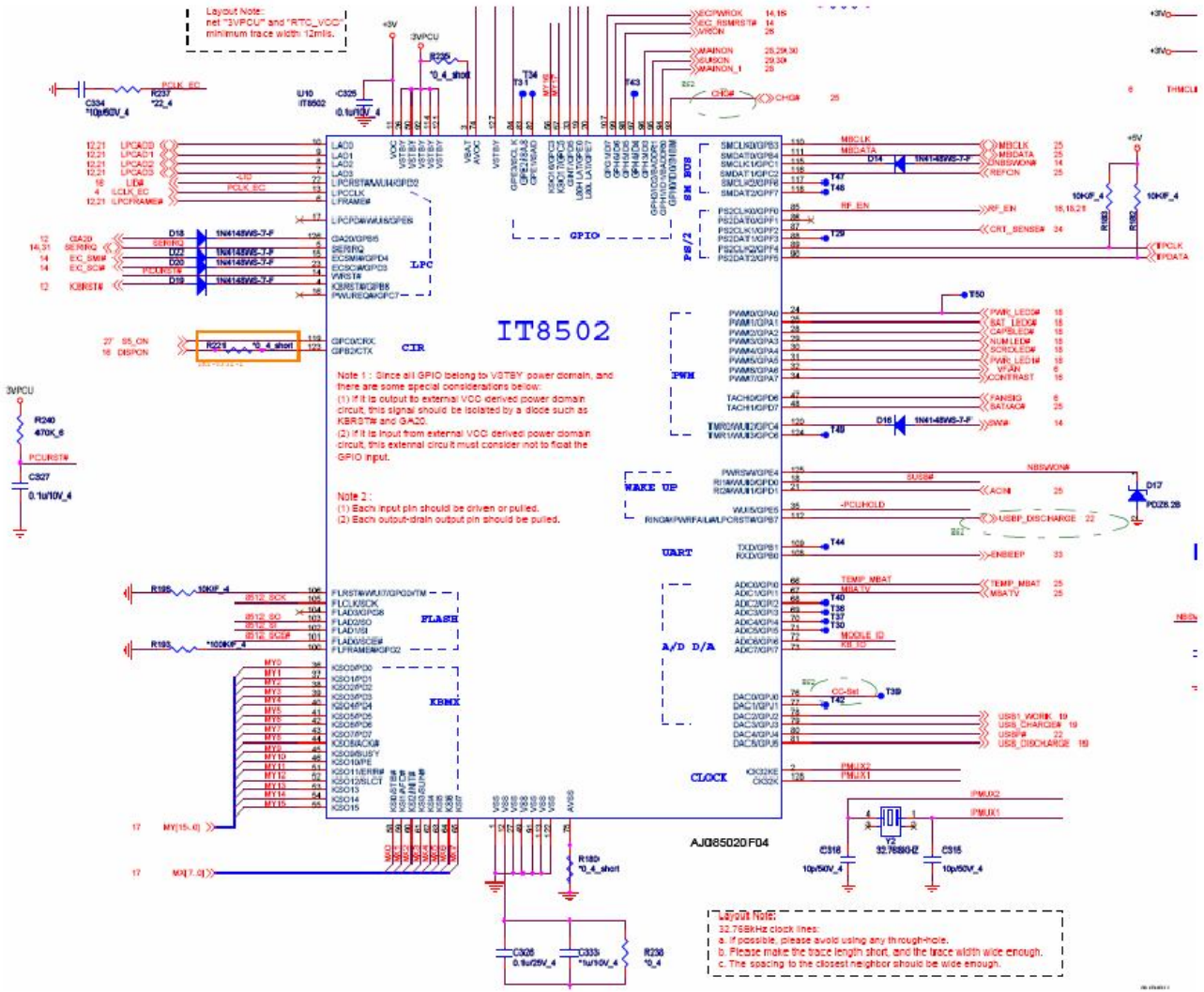

Figure 10-2. Reset Timing

Figure 10-2. Reset Timing

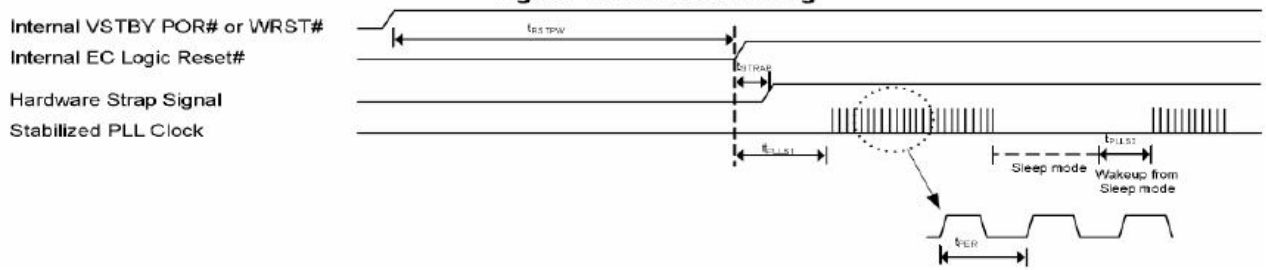

Table 10-2. Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RSTPW}	Internal EC logic reset after VSTBY POR or WRST#	—	1650	—	Tick (by 32.768 KHz)
t_{STRAP}	Strap sampling time	0	—	—	ns
t_{PLLS1}	PLL stabilization time hardware	—	5	—	ms
t_{PLLS2}	PLL stabilization time after waking up from Sleep mode	—	5	—	ms
t_{PER}	PLL clock period	—	$1/_{FreqPLL}$	—	ns
FreqPLL	PLL clock frequency if PLLFREQ = 0011b	—	32.3	—	MHz
	PLL clock frequency if PLLFREQ = 0101b	—	46.0	—	MHz
	PLL clock frequency if PLLFREQ = 0111b	—	64.5	—	MHz
FreqEC	EC clock frequency if PLLFREQ = 0111b	—	9.2	—	MHz